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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Keishi TAMURA et al.
Application No.:	10/769,805
Filed:	February 3, 2004
For:	STORAGE SYSTEM AND STORAGE CONTROLLER
Group:	2186
Examiner:	Not yet assigned

REQUEST FOR RECONSIDERATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

April 20, 2005

Sir:

In response to the Decision on Petition dated March 24, 2005, reconsideration and withdrawal of the Decision is respectfully requested in view of the following remarks.

REMARKS

Initially, in the Decision on Petition dated March 24, 2005, the Examiner notes that the Petition to Make Special filed September 14, 2004 is defective for failing to provide a complete detailed discussion of the most closely related references with the necessary specificity. In addition, the Examiner notes that independent claims 6-9 differ in scope from the discussion presented with respect to independent claims 1 and 2.

The present invention as recited in the claims is directed to, among other things, a storage system constructed by communicably connecting a first storage controller and a second storage controller and performing data processing according to a request from a host device, wherein the first controller has at least one or more logical units accessed by the host device, and at least one or more intermediate memory hierarchies arranged so as to connect this logical unit and at least one or more memory devices, and at least one of the intermediate memory hierarchies is connected to a memory device arranged in the second storage controller.

The present invention as recited in the claims filed are not taught or suggested by any of the above noted references whether taken individually or in combination with each other or in combination with any of the other references now of record.

It is submitted that the cited references, whether considered alone or in combination, fail to disclose or suggest the invention as claimed. In particular, the cited references, at a minimum, fail to disclose or suggest a first storage controller

having at least one or more logical units accessed by a host device, and at least one or more intermediate memory hierarchies arranged so as to connect this logical unit and at least one or more memory devices, and at least one of the intermediate memory hierarchies being connected to a memory device arranged in a second storage controller, and/or obtaining path information to a memory device arranged in said second storage controller, and mapping said obtained path information to an intermediate memory hierarchy connected to a logical unit accessed by said host device, and/or selecting plural paths connected to said external memory device, reading data from said external memory device through each of these selected paths, and judging whether each of these read data is conformed or not, and/or writing separate data different from said read data from one of said selected paths when each of the read data is conformed.

All of the independent claims recite at least one of these features or this feature, if there is only one. In particular, independent claim 1 recites wherein a first storage controller has at least one or more logical units accessed by a host device, and at least one or more intermediate memory hierarchies arranged so as to connect this logical unit and at least one or more memory devices, and at least one of the intermediate memory hierarchies is connected to a memory device arranged in a second storage controller. Independent claim 2 recites at least one or more intermediate memory hierarchies arranged so as to connect said logical unit and at least one or more memory devices, and wherein at least one of the intermediate memory hierarchies is connected to the memory device arranged in the second

storage controller. Independent claim 6 recites obtaining path information to a memory device arranged in said second storage controller; and mapping said obtained path information to an intermediate memory hierarchy connected to a logical unit accessed by said host device. Independent claim 7 recites obtaining path information to the memory device arranged in said second storage controller; and mapping said obtained path information to an intermediate memory hierarchy connected to a logical unit accessed by said host device. Independent claim 8 recites selecting plural paths connected to said external memory device, reading data from said external memory device through each of these selected paths, and judging whether each of these read data is conformed or not. Independent claim 9 recites selecting plural paths connected to said external memory device, reading data from said external memory device through each of these selected paths, judging whether each of these read data is conformed or not, writing separate data different from said read data from one of said selected paths when each of the read data is conformed, again reading data from said external memory device through each of said selected paths, and judging whether these read data are conformed to said separate data or not.

The references considered most closely related to the claimed invention are briefly discussed below:

U.S. Patent No. 5,504,882 (Chai et al.) discloses a fault tolerant disk storage subsystem which includes a multipath dynamically alterable hierarchical

arrangement of storage device controllers. Multiple storage device controllers are provided which are adapted to emulate a storage device and which each include a cache memory which has multiple data input ports and multiple data output ports. A processing element within the storage device controller is utilized to selectively interconnect particular data input ports with selected data output ports to provide multiple paths within the storage device controller. An interconnection is then provided for coupling a data output port of one or storage device controller with a data input port of one more alternate storage device controllers which emulate storage devices, creating an alterable hierarchical arrangement of storage device controllers. Storage devices are then coupled to each of the lowest levels of the hierarchical arrangement of storage device controllers. As the storage device controllers may vary in type and capability, various combinations of access speed and redundancy may be provided. Chai, at a minimum, fails to disclose or suggest a first storage controller having at least one or more logical units accessed by a host device, and at least one or more intermediate memory hierarchies arranged so as to connect this logical unit and at least one or more memory devices, and at least one of the intermediate memory hierarchies being connected to a memory device arranged in a second storage controller, and/or obtaining path information to a memory device arranged in said second storage controller, and mapping said obtained path information to an intermediate memory hierarchy connected to a logical unit accessed by said host device.

U.S. Patent No. 6,073,209 (Bergsten) discloses a computer network comprises a number of storage controllers, each coupled to one of a plurality of storage arrays, each storage array including at least one mass storage device. Each storage controller may be coupled to at least one host processing system and to at least one other storage controller to control access of the host processing systems to the mass storage devices. Multiple copies of data are maintained in storage arrays that are geographically remote to each other, such that any copy can be accessed by any host. Each storage controllers includes an interface with a host that emulates a mass storage device and an interface with a local storage array that emulates a host. The interfaces to the host and local storage arrays are independent of the type of host or devices in the local storage array. Two or more hosts may be dissimilar to each other, and two or more storage arrays may include dissimilar mass storage devices. Hosts access stored data using virtual addressing. During a data access, the storage controller connected to the accessing host maps a virtual address provided by the host to a real physical location in any of the storage arrays, such that the actual location of the data is transparent to the host. The storage controllers provide automatic back-up and error correction as well as write protection of back-up copies. Bergsten, at a minimum, fails to disclose or suggest a first storage controller having at least one or more logical units accessed by a host device, and at least one or more intermediate memory hierarchies arranged so as to connect this logical unit and at least one or more memory devices, and at least one of the intermediate memory hierarchies being connected to a memory device arranged in a second

storage controller, and/or obtaining path information to a memory device arranged in said second storage controller, and mapping said obtained path information to an intermediate memory hierarchy connected to a logical unit accessed by said host device.

U.S. Patent No. 6,295,578 (Dimitroff et al.) discloses a cascaded removable media data storage system includes a first level enhanced removable media data storage system controller connected to a host or server computer network. Connected in parallel to the enhanced first level removable media data storage system controller are at least two enhanced second level removable media data storage system controllers. Each enhanced second level removable media data storage system controllers is connected to a mirrored group of removable media data storage units. Dimitroff et al., at a minimum, fails to disclose or suggest a first storage controller having at least one or more logical units accessed by a host device, and at least one or more intermediate memory hierarchies arranged so as to connect this logical unit and at least one or more memory devices, and at least one of the intermediate memory hierarchies being connected to a memory device arranged in a second storage controller, and/or obtaining path information to a memory device arranged in said second storage controller, and mapping said obtained path information to an intermediate memory hierarchy connected to a logical unit accessed by said host device.

U.S. Patent Publication No. 2003/0221077 (Ohno et al.) discloses a method for controlling a storage system including a host computer, and a first and a

second storage control apparatuses each receiving a data input/output request from the host computer and executing a data input/output process for a storage device in response to the request, comprises connecting a first communication path between the host computer and the first apparatus; connecting a second communication path between the first apparatus and the second apparatus; receiving by the first apparatus a first data input/output request from the host computer through the first path; when the first apparatus has judged that the first request is not for the first apparatus, transmitting by the first apparatus a second data input/output request corresponding to the first request, to the second apparatus through the second path; and by the second apparatus, receiving the second request and executing a data input/output process corresponding to the second request received. Ohno et al., at a minimum, fails to disclose or suggest a first storage controller having at least one or more logical units accessed by a host device, and at least one or more intermediate memory hierarchies arranged so as to connect this logical unit and at least one or more memory devices, and at least one of the intermediate memory hierarchies being connected to a memory device arranged in a second storage controller, and/or obtaining path information to a memory device arranged in said second storage controller, and mapping said obtained path information to an intermediate memory hierarchy connected to a logical unit accessed by said host device.

Therefore, since the references fail to disclose a first storage controller having at least one or more logical units accessed by a host device, and at least one or

more intermediate memory hierarchies arranged so as to connect this logical unit and at least one or more memory devices, and at least one of the intermediate memory hierarchies being connected to a memory device arranged in a second storage controller, and/or obtaining path information to a memory device arranged in said second storage controller, and mapping said obtained path information to an intermediate memory hierarchy connected to a logical unit accessed by said host device, and/or selecting plural paths connected to said external memory device, reading data from said external memory device through each of these selected paths, and judging whether each of these read data is conformed or not, and/or writing separate data different from said read data from one of said selected paths when each of the read data is conformed, it is submitted that all of the claims are patentable over the cited references.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Mattingly, Stanger & Malur, P.C., Deposit Account No. 50-1417 (referencing attorney docket no. 1309.43490X00).

Respectfully submitted,

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